STATIC POWER

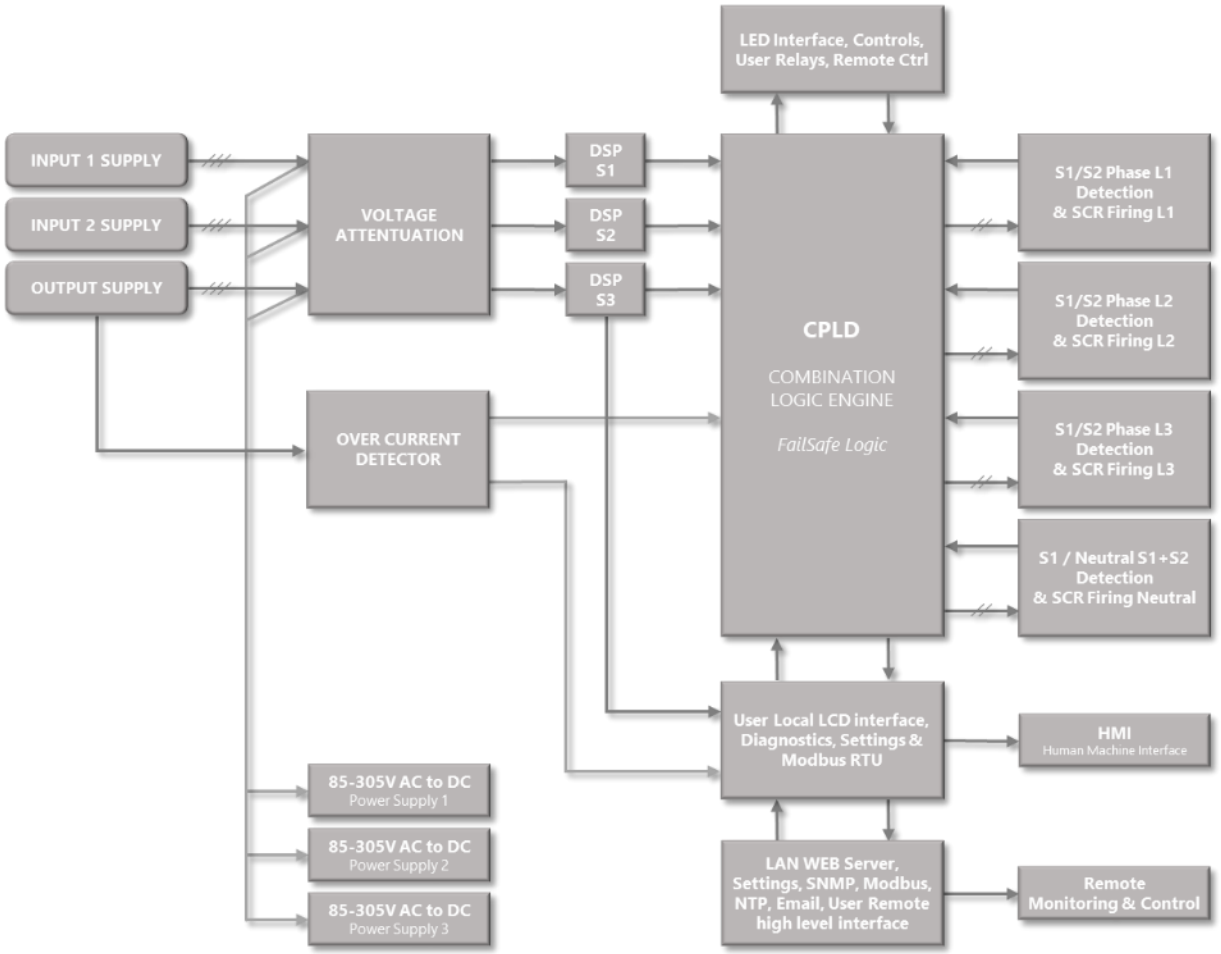
SMART | SOLID | SAFE

FUSELESS iSTS C,H,K & G

How does it work?

iSTS SYSTEM DIAGRAM – iSTS C, H, K & G

iSTS



DETECTION

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The first step of the detection process involves attenuating the three waveforms – Supply 1, Supply 2 and output supply – from the nominal incoming voltage (AC) to 1 Volt (typically).

This provides the STS with the waveforms it requires at a reasonable level for analysis by the three Digital Signal Processors (DSP). Each source has its own DSP and the AC waveforms are continuously sampled at 64 times per cycle and compared to real time maximum and minimum values. On a three-phase system each phase has its own set of 3 inputs and output DSPs.

If an error is detected, for example; 3 consecutive 300µs samples above or below the limit, the DSP returns an output to the CPLD which handles actions. While these transient variations are being monitored, the DSPs are also computing the three supplies RMS values and comparing them to an averaged value, where an output will be returned should any average value fall out of tolerance.

These processes are the same, though independent, for supply 1, supply 2 and output – supply 3. For additional reliability, the supply 3 DSP provides redundant detection for supply 1 and supply 2 and detects power loss at the output in case there is an internal failure. The program in the DSPs are essentially the same and very basic.

ACTION

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Once a fault is identified, a Combinational Programmable Logic Device – CPLD – decides what actions to take and how to perform them.

The CPLD is a fast, simple and reliable hardware digital logic controller which uses combinational logic and a state machine to handle all the actions, sequences and timings required to safely and reliably transfer the connected critical load.

The iSTS is capable of a high-level analysis of power supplies and intelligent interpretation of the results it acquires, however the main switching function is executed through a simple two-step process – detect and act. When the fault signals have been processed and the CPLD has decided what action to take, a signal is sent straight to the switching devices (Thyristors/SCRs).

The CPLD is a digital device that processes many signals and conditions in parallel. Unlike microprocessors, there is no stumbling block for code, stack or program interruption.

REPORTING & MANUAL CONTROL

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Displaying the state of the system brings the user into the picture.

The reporting, where necessary, is achieved by interrogating the “User Local LCD Control Panel”. This is a separate, independent device and does not partake in any control function.

Information gathered by the microprocessor is organized and displayed on the front panel LCD. This information is also made available to the LAN Web Server processor, providing Modbus, SNMP, HTTP, NTP and email alerts which is again separate and plays no part in the operation of the STS, except to provide access for remote interrogation.

The simple display of state through the LED mimic is a more direct process, interfacing only with the CPLD and the reading of registers. This does not interfere with anything else the CPLD or the DSPs may be doing.

With knowledge of the state, the user can manually control the STS. Control pushbuttons, user relays and remote transfer inputs and the LED mimic interface directly with the CPLD, independently from the LCD or any microprocessors. Control inputs from the user can be seen to directly initiate an action in the case of user input or influence an action in the case of fault input.

More involved inputs, such as tolerance settings, are access through the LCD or LAN Web server. Discrete user outputs and inputs (voltage free contacts and remote control inputs) are direct to and from the CPLD.

PROTECTION

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The iSTS Static Transfer Switch incorporates many failsafe measures to ensure reliable operation. The power semiconductors used within the Static Transfer Switches are SCRs - Thyristor modules - and are manufactured by reputable experienced manufacturers like Semikron, a world leader in the supply of power electronic components.

Thyristors/SCRs are very rugged and overrated - typically 2 to 4 times current capacity and typically more than 4 times voltage rating.

The iSTS models C3, H, K and G are a fuseless design and are suitable and safe for installations with fault currents from 20kA to 34kA, depending on the model and options. For installation into higher fault current distributions larger fault current capable Thyristors/SCRs may need to be employed. Larger fault current capability is achieved via the use of large current capable Thyristors/SCRs.

In the absence of fuses these units are rugged enough to clear downstream load faults without Thyristor/SCR failure. Upstream and/or downstream protective systems would clear the fault long before damage to the devices occurs.

In the rare event that one of the SCR/Thyristors fail, the unit incorporates protection circuitry and reporting of SCR/Thyristor failures as Open Circuit or Short Circuit. Even when this occurs your load is fully protected – the functionality of the STS is impaired but not the continuity of power to the load. In fact, there is no logic or process that disrupts power to the load.

PROTECTION

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Events such as over-temperature, overcurrent and overload only raise an alarm. If unattended to a SCR/Thyristor failure may result but this does not result in loss of power to the load.

As well as alarming and recording the Thyristor/SCR fault condition the incoming source breaker will be tripped to isolate the failed device from the source. Any transfer as a result will be transparent to the load.

In the case of a load fault the STS will not transfer to the other source which prevents both sources being affected by the load fault. There may be a loss of power to the connected equipment if the load fault condition has caused the active source to fail, however the source, for example a UPS, is usually able to transfer to its internal bypass and which usually will have the extra capacity to clear the fault.

All other STSs - assuming there are others - will see the transient on the original source and safely transfer to the alternate source without affecting their connected loads.

It is possible although not recommended to isolate the load in case of a fault, but this is not a default operating condition.

Our philosophy is to maintain power to the output of the STS not to disconnect it. Suffice it to say that either mode would be possible.

POWER SUPPLY & REDUNDANCY

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Each unit has a triple redundant power supply module. Only one power supply is required to operate the STS. Power supplies 1, 2, 3 have their own source of AC power which are Input Source 1, Input Source 2 and Output respectively. Each power supply has an extended operating range from 85 to 305VAC and are frequency insensitive.

There are two DC power buses. A 5VDC bus and a 15VDC bus. Backfeed diodes are used to ensure that a failure of one power supply does not cause failure of any other power supply.

Each functionally separate logic block, for example DSPs, CPLD, Display, LAN and I/O, has its own set of regulators to provide a regulated, protected 3.3VDC power bus.

A failure of any functional logic block even if it was affecting its own power supply will not affect anything else and will not cause the STS to malfunction and lose output.

Protection against single points of failure such as this ensure that the STS is always in a safe state and able to continue to supply power to the output.

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